REMARKS

STATUS OF THE CLAIMS

In accordance with the foregoing, no claims are amended for format and formality purposes and no new features for the claimed invention are added. Claims 37-48 were previously cancelled. Claims 3, 9, 10, 21, 27, 28 were previously withdrawn. Claims 1, 2, 4-8, 11-20, 22-26 and 29-36 are pending and under consideration.

No new matter is being presented, and approval of the amended claims is respectfully requested.

REASONS FOR ENTRY

Applicants respectfully request entry of the following arguments because no claim amendments are being presented herein and, therefore, no further search and/or consideration is necessary. It is further submitted that the following remarks may serve to clarify the patentably distinguishable features of the present invention over the cited references.

REJECTIONS OF CLAIMS 1-2, 4-8, 11-13, 15 AND 17 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY LEEDY (U.S. PATENT NO. 5,103,557)

The rejections of claims 1-2, 4-8, 11-13, 15 and 17 are respectfully traversed and reconsideration is requested.

The Examiner states that Leedy discloses detecting, calculating and correcting, as recited in independent claim 1, for example, citing Leedy column 5, line 1, through column 7, line 68, and Figs. 4(a) and 4(b).

Further, in the Response to Arguments, on page 4, item 6, the Examiner states that Leedy discloses an optical aligner and an electrical circuit feedback system that detect the position of an individual electronic component on the semiconductor wafer, and the data of the locations of defective components is used by the CAD to recalculate the locations of the component. The Examiner further states that the CAD holds the displacement data of the good and bad component positions.

However, Applicants respectfully disagree with the Examiner's understanding of Leedy. Leedy discusses merely *aligning* the wafer 1 with the test surface 10, so that the logic units on the wafer 1 can be tested. The results of the test are used to modify a net list to produce a database for the desired interconnect patters on the wafer 1. (See column 5, lines 1-15, and

column 6, lines 45-64). In other words, if a defective integrated circuit logic unit (ICLU) or transistor is found, the interconnects are arranged so as to bypass the defective ICLU and interconnect a defect-free ICLU from the stock of redundant ICLUs. (See Leedy, column 5, lines 33-43).

Leedy further discusses that the wafer 1 and the tester surface 10 are used as an electrical feedback system, which determines the accuracy of the alignment and makes appropriate micron sized adjustments under computer control. Thus, the measurements for the alignment are merely used for adjusting the wafer 1 and the tester surface 10 so that they align properly for testing the ICLUs.

In contrast, some embodiments of the present invention, as recited in independent claim 1, for example, are characterized by calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data, *where the first displacement data is used for correcting design data to be used for processing the board after the board is covered with said first insulating layer.*

Instead, any displacement data obtained in Leedy is merely used to align the wafer 1 with the tester surface 10. Thus, Leedy does not disclose that a displacement is held as first displacement data and, therefore, Leedy fails to teach or even suggest correcting, based on said first displacement data, *design data to be used for processing said board after said board is covered with said first insulating layer*, as recited in independent claim 1, for example.

Moreover, the Examiner states that column 7 of Leedy, in its entirety, discloses E-beams means (maskless), forming vias and additional insulating layers. However, column 7 merely discusses the makeup of tester surface 10 and, therefore, does not relate to the fabrication of a component-embedded board with electronic components, as recited in independent claim 1, for example.

Thus, it is respectfully submitted that independent claim 1, as well as the dependent claims, patentably distinguish over the prior art.

REJECTIONS OF CLAIMS 19-20, 22-26 AND 29-36 UNDER 35 U.S.C. §103(a) AS BEING UNPATENTABLE OVER LEEDY IN VIEW OF KULKARNI ET AL. (U.S. PATENT NO. 5,991,699)

Independent claim 19 recites capturing, before said board is covered with a first insulating layer, an image of a surface of said board on which a first electronic component is formed; calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component detected from first image

data obtained by imaging the surface of said board, and holding said displacement as first displacement data; and correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer.

Therefore, for at least the reasons provided above for independent claim 1, it is respectfully submitted that independent claim 19, as well as the dependent claims, patentably distinguishes over the prior art.

Further, Kulkarni et al. is merely cited as disclosing identifying defects and issuing corrective actions and imaging means. Therefore, it is respectfully submitted that Kulkarni et al. fails to teach or suggest the features of independent claims 1 and 19 described above.

REJECTIONS OF CLAIMS 14, 16 AND 18 UNDER 35 U.S.C. §103(a) AS BEING UNPATENTABLE OVER LEEDY IN VIEW OF KULKARNI ET AL.

Claims 14, 16 and 18 depend from independent claim 1 and inherit the patentability thereof. Thus, it is respectfully submitted that claims 14, 16 and 18 patentably distinguish over the prior art for at least the reasons noted above for claim 1.

Further, as stated above, it is submitted that Kulkarni et al. fails to teach or suggest the features of independent claim 19 and therefore also the similarly-recited features of independent claim 1, as described above.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. Further, all pending claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: October 16, 2006

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